```
=> dis his

     (FILE 'HOME' ENTERED AT 13:05:55 ON 16 OCT 2001)

     FILE 'USPATFULL' ENTERED AT 13:06:05 ON 16 OCT 2001
L1           185 S READ QUEUE#
L2           295 S WRITE QUEUE#
L3          3488 S CACHE# (3A) MISS
L4          3937 S CACHE# (3A) MISS?
L5          3194 S CACHE# (3A) HIT
L6          2369 S L4 AND L5
L7           389 S L1 OR L2
L8            87 S L7 AND L6
L9         10385 S MULTIPROCESS? OR (MULTI (W) PROCESS?)
L10        17573 S PLURAL? (2W) PROCESS?
L11        24325 S L9 OR L10
L12           63 S L11 AND L8
L13        36228 S TAG#
L14           57 S L13 AND L12
L15        27816 S FETCH?
L16           43 S L14 AND L15

=> d 1- pn,ti

YOU HAVE REQUESTED DATA FROM 43 ANSWERS - CONTINUE? Y/(N):y


L16  ANSWER 1 OF 43  USPATFULL
PI     US 6292705          B1   20010918
TI     Method and apparatus for address transfers, system serialization, and
       centralized cache and transaction control, in a symetric
       multiprocessor system

L16  ANSWER 2 OF 43  USPATFULL
PI     US 6240508          B1   20010529
TI     Decode and execution synchronized pipeline processing using decode
       generated memory read queue with stop entry to allow
       execution generated memory read

L16  ANSWER 3 OF 43  USPATFULL
PI     US 6226713          B1   20010501
TI     Apparatus and method for queueing structures in a multi-level
       non-blocking cache subsystem

L16  ANSWER 4 OF 43  USPATFULL
PI     US 6148372               20001114
TI     Apparatus and method for detection and recovery from structural stalls
       in a multi-level non-blocking cache system

L16  ANSWER 5 OF 43  USPATFULL
PI     US 6145054               20001107
TI     Apparatus and method for handling multiple mergeable misses in a
       non-blocking cache

L16  ANSWER 6 OF 43  USPATFULL
PI     US 6032231               20000229
TI     Multiprocessor with split transaction bus architecture
```

providing cache **tag** and address compare for sending retry direction to other bus module upon a match of subsequent address bus cycles to content of cache **tag**

L16 ANSWER 7 OF 43 USPATFULL
PI US 5854913 19981229
TI Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures

L16 ANSWER 8 OF 43 USPATFULL
PI US 5822611 19981013
TI Method for cycle request with quick termination without waiting for the cycle to reach the destination by storing information in queue

L16 ANSWER 9 OF 43 USPATFULL
PI US 5809320 19980915
TI High-performance **multi-processor** having floating point unit

L16 ANSWER 10 OF 43 USPATFULL
PI US 5732244 19980324
TI **Multiprocessor** with split transaction bus architecture for sending retry direction to other bus module upon a match of subsequent address bus cycles to content of cache **tag**

L16 ANSWER 11 OF 43 USPATFULL
PI US 5701502 19971223
TI Isolating a central processing unit from the operating system controlling said unit and its associated hardware for interaction of the unit with data handling apparatus alien to the operating system

L16 ANSWER 12 OF 43 USPATFULL
PI US 5542058 19960730
TI Pipelined computer with operand context queue to simplify context-dependent execution flow

L16 ANSWER 13 OF 43 USPATFULL
PI US 5488730 19960130
TI Register conflict scoreboard in pipelined computer using pipelined reference counts

L16 ANSWER 14 OF 43 USPATFULL
PI US 5481689 19960102
TI Conversion of internal processor register commands to I/O space addresses

L16 ANSWER 15 OF 43 USPATFULL
PI US 5471591 19951128
TI Combined write-operand queue and read-after-write dependency scoreboard

L16 ANSWER 16 OF 43 USPATFULL
PI US 5450555 19950912
TI Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions

L16 ANSWER 17 OF 43 USPATFULL
PI US 5432918 19950711
TI Method and apparatus for ordering read and write operations using conflict bits in a **write queue**

L16 ANSWER 18 OF 43 USPATFULL
PI US 5418973 19950523
TI Digital computer system with cache controller coordinating both vector

and scalar operations

L16 ANSWER 19 OF 43 USPATFULL
PI US 5404483 19950404
TI Processor and method for delaying the processing of cache coherency transactions during outstanding cache fills

L16 ANSWER 20 OF 43 USPATFULL
PI US 5404482 19950404
TI Processor and method for preventing access to a locked memory block by recording a lock in a content addressable memory with outstanding cache fills

L16 ANSWER 21 OF 43 USPATFULL
PI US 5394529 19950228
TI Branch prediction unit for high-performance processor

L16 ANSWER 22 OF 43 USPATFULL
PI US 5388215 19950207
TI Uncoupling a central processing unit from its associated hardware for interaction with data handling apparatus alien to the operating system controlling said unit and hardware

L16 ANSWER 23 OF 43 USPATFULL
PI US 5369767 19941129
TI Servicing interrupt requests in a data processing system without using the services of an operating system

L16 ANSWER 24 OF 43 USPATFULL
PI US 5369749 19941129
TI Method and apparatus for the direct transfer of information between application programs running on distinct processors without utilizing the services of one or both operating systems

L16 ANSWER 25 OF 43 USPATFULL
PI US 5363497 19941108
TI System for removing section of memory from first system and allocating to second system in a manner indiscernable to both operating systems

L16 ANSWER 26 OF 43 USPATFULL
PI US 5347648 19940913
TI Ensuring write ordering under writeback cache error conditions

L16 ANSWER 27 OF 43 USPATFULL
PI US 5333296 19940726
TI Combined queue for invalidates and return data in **multiprocessor** system

L16 ANSWER 28 OF 43 USPATFULL
PI US 5325517 19940628
TI Fault tolerant data processing system

L16 ANSWER 29 OF 43 USPATFULL
PI US 5317720 19940531
TI Processor system with writeback cache using writeback and non writeback transactions stored in separate queues

L16 ANSWER 30 OF 43 USPATFULL
PI US 5283868 19940201
TI Providing additional system characteristics to a data processing system through operations of an application program, transparently to the operating system

L16 ANSWER 31 OF 43 USPATFULL
PI US 5155843 19921013

TI Error transition mode for **multi-processor** system

L16 ANSWER 32 OF 43 USPATFULL
PI US 5155809 19921013
TI Uncoupling a central processing unit from its associated hardware for interaction with data handling apparatus alien to the operating system controlling said unit and hardware

L16 ANSWER 33 OF 43 USPATFULL
PI US 5144692 19920901
TI System for controlling access by first system to portion of main memory dedicated exclusively to second system to facilitate input/output processing via first system

L16 ANSWER 34 OF 43 USPATFULL
PI US 5113522 19920512
TI Data processing system with system resource management for itself and for an associated alien processor

L16 ANSWER 35 OF 43 USPATFULL
PI US 4636946 19870113
TI Method and apparatus for grouping asynchronous recording operations

L16 ANSWER 36 OF 43 USPATFULL
PI US 4633387 19861230
TI Load balancing in a multiunit system

L16 ANSWER 37 OF 43 USPATFULL
PI US 4583166 19860415
TI Roll mode for cached data storage

L16 ANSWER 38 OF 43 USPATFULL
PI US 4533995 19850806
TI Method and system for handling sequential data in a hierarchical store

L16 ANSWER 39 OF 43 USPATFULL
PI US 4525780 19850625
TI Data processing system having a memory using object-based information and a protection scheme for determining access rights to such information

L16 ANSWER 40 OF 43 USPATFULL
PI US 4493027 19850108
TI Method of performing a call operation in a digital data processing system having microcode call and return operations

L16 ANSWER 41 OF 43 USPATFULL
PI US 4455602 19840619
TI Digital data processing system having an I/O means using unique address providing and access priority control techniques

L16 ANSWER 42 OF 43 USPATFULL
PI US 4445177 19840424
TI Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions

L16 ANSWER 43 OF 43 USPATFULL
PI US 4403288 19830906
TI Methods and apparatus for resetting peripheral devices addressable as a plurality of logical devices

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L14           57 S L13 AND L12
L15        27816 S FETCH?
L16           43 S L14 AND L15
L17           91 S L1 AND L2
L18           20 S L6 AND L17
L19           14 S L11 AND L18
L20           11 S L19 AND L13
L21            6 S L15 AND L20
                 SAVE ALL C212291/L
L22          251 S TRANSACTION? QUEUE?
L23           22 S L6 AND L22
L24          126 S L11 AND L22
L25           13 S L11 AND L23
L26           12 S L13 AND L25
L27            9 S L15 AND L26

=> dis 1- pn,ti

YOU HAVE REQUESTED DATA FROM 9 ANSWERS - CONTINUE? Y/(N):y


L27  ANSWER 1 OF 9  USPATFULL
PI     US 6298418          B1   20011002
TI     Multiprocessor system and cache coherency control method

L27  ANSWER 2 OF 9  USPATFULL
PI     US 6272602          B1   20010807
TI     Multiprocessing system employing pending tags to
       maintain cache coherence

L27  ANSWER 3 OF 9  USPATFULL
PI     US 6269427          B1   20010731
TI     Multiple load miss handling in a cache memory system

L27  ANSWER 4 OF 9  USPATFULL
PI     US 6237059          B1   20010522
TI     Method for estimating statistics of properties of memory system
       interactions among contexts in a computer system

L27  ANSWER 5 OF 9  USPATFULL
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PI US 6202127 B1 20010313
TI Apparatus for spatial and temporal sampling in a computer memory system

L27 ANSWER 6 OF 9 USPATFULL
PI US 6195748 B1 20010227
TI Apparatus for sampling instruction execution information in a processor pipeline

L27 ANSWER 7 OF 9 USPATFULL
PI US 6026461 20000215
TI Bus arbitration system for **multiprocessor** architecture

L27 ANSWER 8 OF 9 USPATFULL
PI US 5887146 19990323
TI Symmetric **multiprocessing** computer with non-uniform memory access architecture

L27 ANSWER 9 OF 9 USPATFULL
PI US 5657472 19970812
TI Memory transaction execution system and method for **multiprocessor** system having independent parallel **transaction queues** associated with each processor